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10/587,596	04/24/2007	Wolfgang Schnitt	DE04 0034 US1	2386

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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
05/14/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,596	SCHNITT ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 27, 2008 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kalnitsky (US 5,786,613). **Kalnitsky discloses an integrated circuit chip** (e.g. figures 3, 8, and 9), **comprising in sequence,**

a substrate layer of a substrate material (substrate 21),

an insulating layer of an electrically insulating material (e.g. insulating layer 34, disclosed in col. 5, line 20),

a first electrically conductive layer of a first electrically conductive material (electrically conductive layer 60, disclosed in col. 6, lines 7 – 8),

a dielectric layer of a dielectric material (dielectric layer 46, disclosed in col. 5, line 43) **and**

a second electrically conductive layer of a second electrically conductive material (e.g. second conductive layer 42, disclosed in col. 5, line 28),

said IC chip comprising at least one integrated circuit and at least one integrated electrostatic discharge protection device (e.g. integrated circuit disclosed in col. 5, lines 11 - 17, and electrostatic discharge device disclosed in col. 2, lines 60 - 62 and col. 7, lines 27 - 31), **said electrostatic discharge protection device comprising,**

a pair of spaced center and circumferential electrodes (center electrode 60 and circumferential electrode formed by layer 42, as disclosed in col. 6, line 65 - col. 7, line 1)**, the center electrode being formed by the first electrically conductive layer and the circumferential electrode being formed by the second electrically conductive layer** (as disclosed in col. 6, line 65 - col. 7, line 1), **said electrodes being separated by a toroidal spark gap cavity** (cavity 68, as seen in figures 8 and 9, and disclosed in col. 6, line 49), **wherein the toroid of the toroidal spark gap cavity comprises,**

a base layer formed by the insulating layer of the integrated circuit chip (e.g. layer 34 forms a layer around the base of the gap, as seen in figure 8),

a side wall formed by the circumferential electrode (e.g. as seen in figure 8, the upper portion of the gap has a side wall formed by the circumferential electrode 42),

a cover layer formed entirely by the dielectric layer of the integrated circuit chip (e.g. as seen in figure 8, dielectric layer 46 covers the circumferential electrode 42 and top side of the gap 68, and therefore may be considered as a "cover layer"), **and the center of the toroid being formed by the center electrode comprising a contact pad in contact with the insulating layer** (e.g. as seen in figure 8, contact pad formed by layer 58 at the center of the toroid is in contact with the insulating layer 34),

said electrostatic discharge protection device also comprising means to electrically connect the center electrode to input circuit paths to be protected from electrostatic discharge (e.g. conductive layer 66 may be considered a means to electrically connect the center electrode to an input circuit path since it is capable of this function. Furthermore, while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See MPEP 2114. Furthermore, it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114) **and means to electrically connect the circumferential electrode to an electrostatic discharge path comprising either a connection to a circuit ground or a circuit supply voltage** (e.g. conductive layer 67 may be considered a means to electrically connect the circumferential electrode to an electrostatic discharge path comprising a circuit ground or supply voltage since it is

capable of this function. Furthermore, while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997). See MPEP 2114. Furthermore, it has been held by the courts that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham 2 USPQ2d 1647 (1987). See MPEP 2114).

4. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by El-Kareh et al. (US 5,933,718, prior art of record). **El-Kareh discloses a method of fabricating an integrated circuit chip comprising an integrated circuit and an electrostatic discharge protection device** (e.g. see figures 1A - 1E and 2) **comprising the steps of**

a) **providing a semiconductor substrate** (substrate 10),

b) **depositing an insulating layer on the semiconductor substrate** (gate oxide 151 col. 1, line 56),

c) **depositing a first electrically conductive layer of a first electrically conductive material on said insulating layer** (polysilicon layer 152, col. 1, line 56),

d) **depositing a dielectric layer of a dielectric material directly on said first electrically conductive layer** (insulating layer 258, col. 2, line 8, directly on the side of the first electrically conductive layer 152),

e) **etching spaced contact windows for a center electrode** (etched window 100, shown in figure 1B, as discussed in col. 2, lines 25 - 26) **and a circumferential electrode** (window 211 of figure 1D, as discussed in col. 2, lines 59 - 63),

f) **depositing a mask** (e.g. col. 2, lines 32 – 35 discuss the conventional use of blocking parts of the device with photoresist, which is a mask, and col. 2, lines 1 -2, discuss the use of photoresist to selectively remove materials),

g) **etching a hollow groove into the first electrically conductive layer under the circumference of the contact window of the circumferential electrode** (e.g. figure 1B shows groove 112 formed into the first conducting layer 152, which is formed by etching, as discussed in col. 2, lines 26 – 50),

h) **depositing a layer of a second electrically conductive layer** (e.g. figure 2, layer 170 and 178, which is formed simultaneously, as discussed in col. 3, lines 26 – 27, and are made of a conductor, as discussed in col. 2, line 67 through col. 3 line 2) **through the contact window of the center electrode to mechanically contact the insulating layer** (e.g. figure 2 shows the conducting layer 170 in mechanical contact to the oxide layer 151, via the oxide layer 153. Layer 153 is discussed in col. 2, lines 51 – 56)), **and through the contact window of the circumferential electrode to electrically contact the first electrically conductive layer** (e.g. figure 2 shows layer 178 in the contact window of the circumferential electrode that is electrically in contact to the first electrically conductive layer 152 via the conductive layer 154. Conductive layer 154 is discussed in col. 1, line 57), and

i) **connecting the center electrode to input circuit paths to be protected from electrostatic discharge** (e.g. line 3 discloses that center electrode 170 is connected to ground. Electrons travel from negative (ground) to positive, so that the input of the signal is from ground (negative)) **and connecting the circumferential electrode to an electrostatic discharge path comprising either a connection to a circuit ground or a circuit supply voltage** (e.g. figure 2 shows the circumferential electrode 178 connected to the circuit, which necessarily must contain either a circuit supply or circuit ground for current to flow).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2, 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kalnitsky in view of Momodomi (US 4,881,113, prior art of record).

a. Regarding claim 2, **Kalnitsky discloses the integrated circuit chip of claim 1, as cited above, but is silent with respect to explicitly disclosing the integrated circuit chip further comprises a passive component selected from the group comprising resistors, capacitors, and inductors.**

Momodomi discloses that an integrated circuit chip may comprise passive components selected from the group comprising resistors, capacitors, and inductors (e.g. figures 4a and 4b show the equivalent circuit of figures 2a and 2b, as discloses in col. 4, lines 12 - 16, which shows a resistor in the circuit).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kalnitsky such that the integrated circuit chip discloses passive components since Kalnitsky discloses the integrated circuit chip to comprise various transistors (col. 5, line 13) and an electrostatic discharge device, and it is well-known in the art that integrated circuit chips also comprises various passive components, as further taught by Momodomi. One would have been motivated to include various passive components in the integrated circuit chip of Kalnitsky since such passive components are necessary in creating various circuits in electronic designs, such as amplifiers, filters, etc...

b. Regarding claim 4, **Kalnitsky discloses the integrated circuit chip of claim 1, but is silent with respect to disclosing that the second electrically conductive material is aluminum. However, Kalnitsky discloses that other conductive layers may comprise aluminum** (col. 6, lines 59 - 60).

Furthermore, Momodomi discloses an integrated circuit chip may comprise electrically conductive material is aluminum (col. 3, lines 1 – 2 disclose the second electrode 18 to be aluminum Al. Col. 6, lines 30 – 32 also disclose that it may be made from Mo and W instead of Al).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kalnitsky such that the second conductive layer was formed of aluminum since Kalnitsky discloses the layer to be conductive, but is simply silent with respect to the material, and both Kalnitsky and Momodomi disclose that aluminum may be used as conductive layers in integrated circuit devices. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use aluminum as the second conductive layer material since it is very conductive, inexpensive, and may be formed using predictable, known methods such as evaporation.

c. Regarding claim 6, **Kalnitsky discloses the integrated circuit chip of claim 1, as cited above, but is silent with respect to explicitly disclosing the substrate material is selected from the group comprising silicon, glass and a ceramic material**. However, Kalnitsky discloses that transistors are formed in the substrate (e.g. as seen in figure 3, and disclosed in col. 5, lines 11 - 13).

Momodomi discloses an integrated circuit chip, wherein the substrate material is selected from the group comprising silicon, glass and a ceramic material (col. 2, line 64 discloses the substrate to be made of silicon).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Kalnitsky such that the substrate is formed of silicon since Kalnitsky discloses the substrate to comprise transistors, and it is well-known in the art that transistors and other integrated circuits may be formed in silicon substrates, as further supported by Momodomi. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use silicon as a substrate since it was a well-known, inexpensive material that is semiconducting and allows one to form integrated circuits on readily and with well-known methods.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kalnitsky in view of Chen et al. (US 5,656,534, prior art of record). **Kalnitsky discloses the**

integrated circuit chip of claim 1, as cited above, but is silent with respect to the first electrically conductive material being made of polysilicon.

Chen teaches that an electrically conductive layer forming a polysilicon electrode may be used in electrostatic discharge (ESD) devices (col. 2, line 41, and col. 3, lines 38 – 40, and layer 34 of ESD device shown in figure 1).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to form the integrated circuit chip of Kalnitsky such that the center electrode is made of polysilicon, since Kalnitsky discloses the center electrode to be made of a conductive material, and Chen discloses that electrodes for ESD devices may be formed of polysilicon. Furthermore, it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would be motivated to make an electrode of polysilicon since its properties are well-known in the art and reliable, as discussed by Chen (Background of Invention).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kalnitsky in view of Igel et al. (US 6,204,549 B1, prior art of record). **Kalnitsky discloses the integrated circuit chip of claim 1, as cited above, wherein the spark gap cavity contains a gas for reducing the breakdown voltage of the electrostatic discharge protection device** (col. 6, lines 49 - 50). **Kalnitsky is silent with respect to disclosing the gas is a noble gas.**

Igel teaches that a cavity filled with a noble gas may be used in voltage protection devices (col. 2, lines 38 – 40).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the spark gap cavity of Kalnitsky such that it is filled with a noble gas, since Kalnitsky discloses the gap to contain a gas, and Igel teaches that noble gas filled cavities can be used in between electrodes in protection devices. One would be motivated to make such a modification since a noble gas filled cavity allows one to control the breakdown voltage between the electrodes, as discussed by Igel (col. 2, lines 44 – 47), as well as not being reactive with the electrodes so that there is no corrosive effects.

Response to Arguments

10. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection. As cited above with respect to claim 1, the prior art of Kalnitsky discloses the structural limitations as recited by the claim and as broadly interpreted by the examiner per MPEP 2111. With respect to the interpretation of the "*base layer*" and "*cover layer*", neither layer has been recited such that the term "*base*" and "*cover*" positively and distinctly determines the location of the layer. As discussed above with respect to claim 1, the layer 34 may be considered as a "*base layer*" since it surrounds the spark cavity gap at the bottom of the gap. Layer 46 may be considered a "*cover layer*" since it both covers the circumferential electrode layer 42 as

well as covering the top sides of the spark cavity gap. Therefore, the claimed invention is anticipated by Kalnitsky.

11. Applicant's arguments with respect to claim 7 filed on October 27, 2008 have been fully considered but they are not persuasive in view of the new interpretation of the prior art of El-Kareh et al. At present, the prior art of El-Kareh remains commensurate to the scope of the claims as stated by the Applicant within the context of the claim language and as broadly interpreted by the Examiner [MPEP 2111], which is elucidated and expounded upon above. In response to Applicants arguments drawn to the amendment, "*depositing a dielectric layer of dielectric material directly on said first electrically conductive layer*", the prior art of El-Kareh discloses in figure 1A that an insulating layer 258 (disclosed in col. 2, line 8) may be deposited directly on the side of electrically conductive layer 152, as seen in the figure. It is well-known that a dielectric layer may also be considered an insulating (non-conductive) layer. Therefore, El-Kareh anticipates the claimed limitations, as cited above with respect to claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
May 4, 2009